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by

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A PULSE HEIGHT ANALYZER WITH AUTOMATIC DIFFERENTIAL DEADTIME CORRECTION*

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ABSTRACT

A 4096 channel pulse height analyzer is described that features automatic differential deadtime correction of spectra at input rates up to 5×10^4/sec.

1. Introduction

The increasing use of pulse height analysis in research programs at the Savannah River Laboratory (SRL), combined with the decreasing prices of semiconductor memory chips, made it feasible to design a pulse height analyzer (PHA) that fulfills our specialized needs. These needs are: (1) computer control capability, (2) low resolution degradation at count rates up to 5×10^4/sec, and (3) capability to measure short half-life isotopes with minimal spectrum distortion due to deadtime.

2. Analog-to-Digital Converter (ADC)

The ADC is similar to a design by Westphal[1,2]. A block diagram of the ADC is shown in fig. 1. The linear signal from

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the pulse amplifier is delayed for 2 microseconds while the undelayed signal is inspected for appropriate amplitude limits and absence of pileup. If the requirements are met, a conversion command is generated in the control logic. The leading edge of the conversion command resets the successive approximation converter (SAC), and the trailing edge starts the conversion. The busy signal from the SAC is used to switch the sample-hold from "track" to "hold" mode. The feedthrough from the sample-hold is low enough that a linear gate is unnecessary. The sliding scale averaging technique[3]) is implemented with a 7-bit counter, a 10-bit digital-to-analog converter (DAC) of which only the 7 high order bits are used, and a 12-bit subtractor.

The trailing edge of every STORE pulse advances the 7-bit counter, whose digital outputs are connected to the DAC and one input set of the subtractor. The analog output of the DAC is attenuated and applied to the comparator of the SAC unit. At the conclusion of the conversion, the BUSY signal from the SAC unit returns to logic zero which generates the STORE command. STORE is used to gate the 12-bit word from the SAC unit to the other input set of the subtractor. The actual subtraction takes place during the first 60 nanoseconds of the STORE command, and the resulting 12-bit address is latched into the memory address register 200 nanoseconds later.

Several commercial SAC units have been used in this design with conversion times ranging from 3.5 to 25 microseconds. The differential linearity of unselected SAC units is rather poor

and results in a differential linearity for the ADC of approximately 3%. Selection of SAC units for this parameter can improve this linearity by an order of magnitude. A further improvement can be made by using only the 12 most significant bits of a 13- or 14-bit SAC. This results in a longer conversion time, however.

3. Automatic Differential Deadtime Correction

A significant departure from usual practice in this PHA is that ADD1 pulses to the memory unit are generated by a threshold detector circuit operating directly on the preamplifier output, which issues a standardized pulse for every event over the noise level. By counting these pulses between successive digitizations and adding the resulting number to the contents of the address next produced by the ADC, automatic differential deadtime correction is achieved. This method is an adaptation of a scheme by J. Harms[4]), and the reader is referred to his paper for a mathematical analysis. The deadtime correction register is contained in the memory unit. The standardized threshold detector pulses are also used as the input signals to the pileup detector[5]) circuits.

4. Memory Controller (fig. 2)

The PHA memory section is controlled with a pulse asynchronous sequential logic circuit (fig. 3). Inputs are ADD1, STORE, MODE, and 10 MHz CLK. ADD1 and STORE were described in the previous sections. The controller is enabled to analyze PHA events with MODE. Pulses to alter data from the PHA memory are derived from 10 MHz CLK (a 10^7 pps clock pulse train).

A STORE pulse from the ADC initiates the one-microsecond (nominal) read/alter/write memory cycle. At the beginning of the alter part of the memory cycle, the DEADTIME correction MODULO-4 counter contains a positive binary number representing the number of ADD1 events received from the ADC since the previous alter operation. During alter, the ADD1 events are inhibited with a BUSY flip-flop at the input to DEADTIME correction register and steered to a MEMORY BUSY MODULO-2 counter. This counter will accumulate up to two counts that may be issued by the ADC during the memory alter operation that requires nominally 0.2 to 0.5 microsecond. The memory thus contributes "zero deadtime" to the PHA operation. The ALTER MEMORY pulse train increments the MEMORY DATA register (fig. 3) once for each ADD1 event stored in the DEADTIME correction register, and at the same time decrements that register until its borrow output clears BUSY flip-flop to terminate the memory alter operation. At that time, the altered memory data for the location addressed by the 12-bit ADC data are stored in the solid-state 4096 × 20-bit array. The DEADTIME correction register is initialized with the binary number stored in the MEMORY BUSY counter, and the memory cycle is repeated until the PHA is switched from ANALYZE mode.

A memory READOUT mode allows external pulses to control the memory cycle through an I/O (input/output) interface connector on the rear of the NIM module. The MEMORY ADDRESS counter is set to zero and then incremented after a read/write memory cycle. Memory data in 20-bit binary format are available through the I/O connector.

The PHA operating in its AUTO mode can be easily interfaced for remote operation by a computer or any other type of automatic data acquisition system. A memory clearing operation may be remotely triggered, or operated by a manual pushbutton, to clear the 4096 memory locations in 410 milliseconds. In AUTO, a microprocessor-based Serial Output Module[6]) will control the PHA with a 110-baud serial typewriter terminal or a 2400-baud serial full-duplex communications channel.

A DISPLAY mode provides interfacing to a remote digital display package[7]) for viewing PHA spectra on an ordinary laboratory oscilloscope.

5. Performance of the PHA

The performance of the PHA was tested with an intrinsic germanium detector, an ORTEC Model 471 pulse amplifier, and ^{137}Cs, ^{22}Na, and ^{60}Co sources. The ^{137}Cs source was placed in a fixed position relative to the detector, and the ^{22}Na and ^{60}Co sources were used independently and in combination to create the different conditions of total counting rate and spectral composition. Table 1 shows the result of these tests. Fig. 4 shows some of the results in graphic form and demonstrates the insensitivity of the counts in the ^{137}Cs peak (FW 0.1M) versus total count rate over the range from 10^3 to 5×10^4 per second. The decrease in the region 10^4 to 3×10^4 counts per second is due to a complex interaction between the baseline restorer in the pulse amplifier and the peak detector following overload pulses. The decrease at 5×10^4 counts

per second is due partially to the deadtime of the threshold detector, which is energy dependent but has a value of approximately 0.5 microsecond for ^{60}Co full energy events. Above 5×10^4 counts per second, the capacity of the deadtime correction register is exceeded and causes further loss of counts. A logic analyzer connected to this register produced the data (Table 2) that show the rate (r) of occurrence of the storage of n ($1 > n > 15$) counts at several different total count rates. The deadtime correction register is connected so that if it reaches a count of "15" it remains there until it is "read" instead of "wrapping around." This explains why "15" occurs more often than "14" at high count rates.

6. Conclusions

A hardware method for the realization of a PHA with automatic differential deadtime correction up to input rates of 5×10^4/sec has been shown. The technique could be extended to higher input rates by increasing the size of the deadtime correction register. The ultimate limit is set by the time resolution of the threshold detector circuit.

References

[1]) G. P. Westphal, Nucl. Instr. and Meth. 113 (1973) 77.

[2]) G. P. Westphal, Nucl. Instr. and Meth. 136 (1976) 271.

[3]) C. Cottini, E. Gatti and V. Svelto, Nucl. Inst. and Meth. 24 (1964) 241.

[4]) J. Harms, Nucl. Instr. and Meth. 53 (1967) 192.

[5]) C. J. Daniels, Rev. Sci. Inst. 46(1) (1975) 102.

[6]) J. S. Byrd, "A microprocessor-based controller for nuclear instruments" (submitted for publication in IEEE Transactions on Nuclear Science).

[7]) W. J. Woodward, Savannah River Laboratory (to be published).

TABLE 1

Counting rate and spectral composition. All data taken from spectra collected for 600 seconds, clock time.

Source	Conversions (STORE) per second	Events (ADD1) per second	Counts under peak	Resolution (FW 0.1M), keV
^{137}Cs	1519 ±12	1570 ±12	135374 ±368	3.0
$^{137}Cs + ^{22}Na + ^{60}Co$	4618 ±21	5069 ±22	134820 ±372	3.1
$^{137}Cs + ^{22}Na + ^{60}Co$	9177 ±30	10808 ±33	133430 ±371	3.1
$^{137}Cs + ^{60}Co$	15360 ±39	20282 ±45	131140 ±395	3.13
$^{137}Cs + ^{22}Na$	18375 ±43	26526 ±51	131342 ±380	3.19
$^{137}Cs + ^{60}Co$	18718 ±43	26826 ±52	131499 ±408	3.22
$^{137}Cs + ^{60}Co$	21976 ±47	35756 ±60	133763 ±431	3.35
$^{137}Cs + ^{60}Co$	24807 ±50	46579 ±68	133389 ±452	3.48
$^{137}Cs + ^{60}Co$	27577 ±52	65424 ±81	125832 ±475	3.53

TABLE 2

Storage of n counts at different total input rates

n	1605 counts/sec r	1605 counts/sec n x r	21660 counts/sec r	21660 counts/sec n x r	47038 counts/sec r	47038 counts/sec n x r	65770 counts/sec r	65770 counts/sec n x r
1	1423	1423 ±12	11861	11861 ±34	13214	13214 ±36	11620	11620 ±34
2	66.8	134 ±1.6	2362	4724 ±31	5447	10894 ±47	6376	12752 ±50
3	17.3	52 ±1.3	913	2739 ±29	2589	7767 ±48	3376	10128 ±55
4	2.3	9 ±0.6	307	1228 ±22	1332	5328 ±46	2045	8180 ±57
5	0.5	3 ±0.35	112	560 ±17	718	3590 ±42	1255	6275 ±56
6			41.6	250 ±3.9	404	2424 ±38	798	4788 ±54
7			14.6	102 ±2.7	208	1456 ±32	498	3486 ±49
8			5.9	47 ±1.9	113	904 ±27	309	2472 ±44
9			2.0	18 ±1.3	61.9	557 ±7	187	1683 ±39
10			0.6	6 ±0.8	34.1	341 ±5.8	122	1220 ±35
11					18.2	200 ±4.7	78.4	862 ±9.7
12					10.5	126 ±3.9	50.1	601 ±8.5
13					5.0	65 ±2.9	30.8	400 ±7.2
14					3.0	42 ±2.4	19.4	272 ±6.2
15					3.5	53 ±2.8	32.6	489 ±8.6
Total		1621 ±12		21535 ±61		46960 ±114		65229 ±153

LIST OF FIGURES

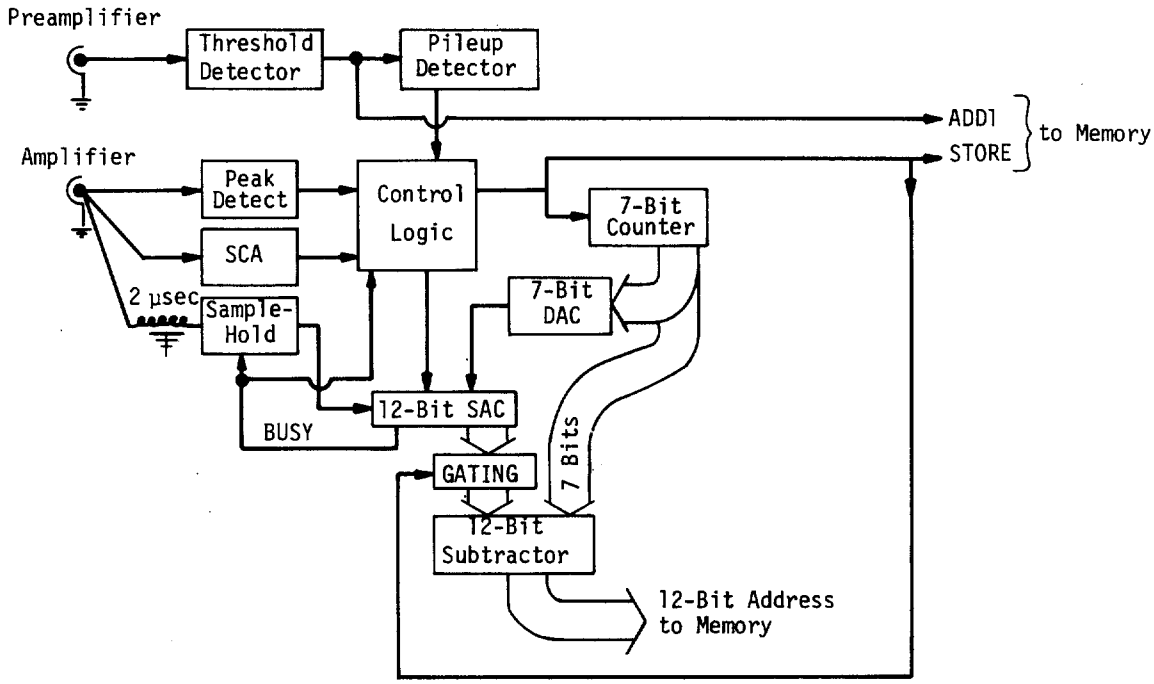

Fig. 1. Block diagram of ADC.

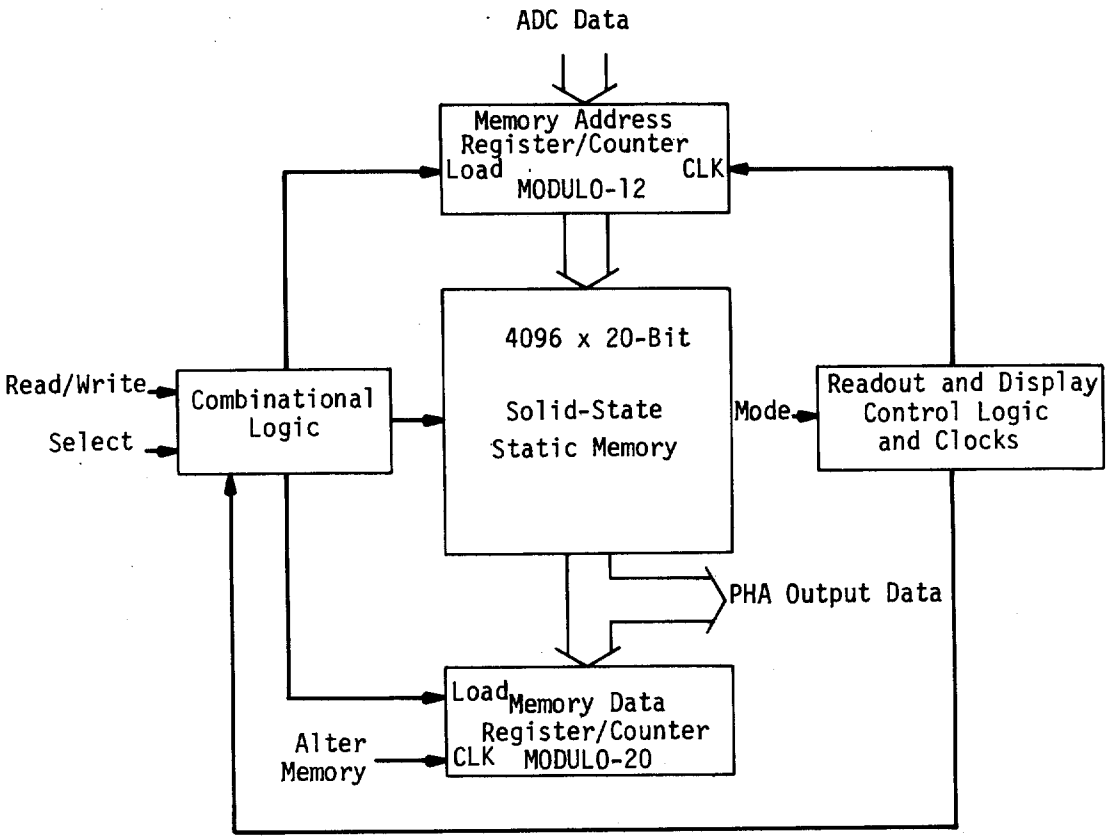

Fig. 2. Block diagram of memory.

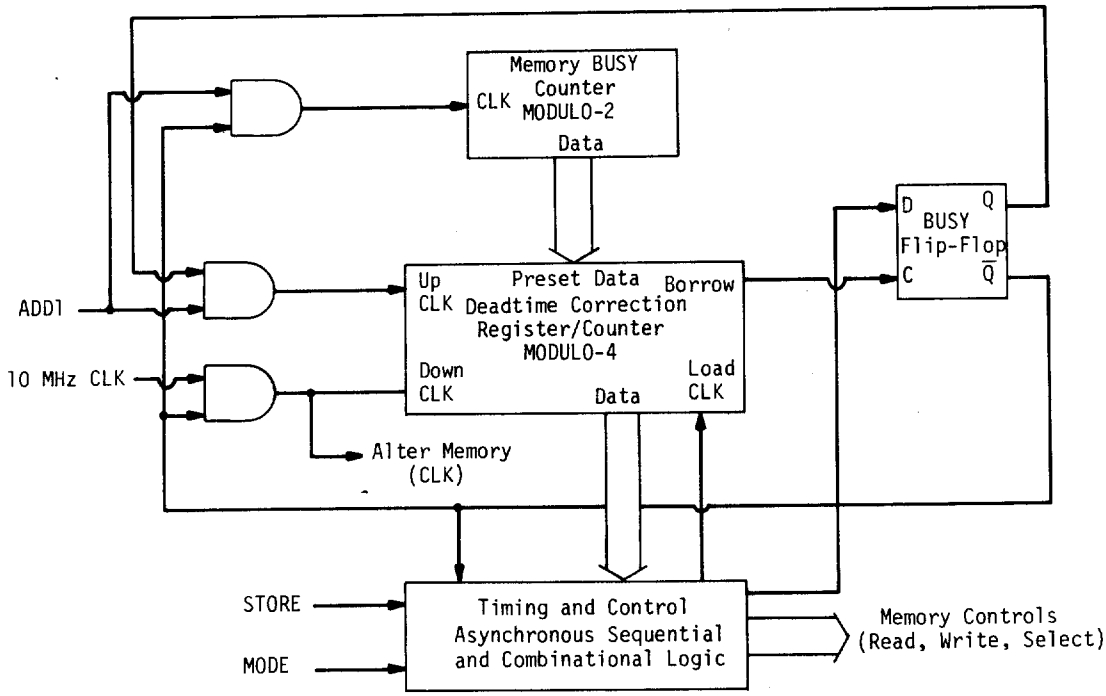

Fig. 3. Memory control diagram.

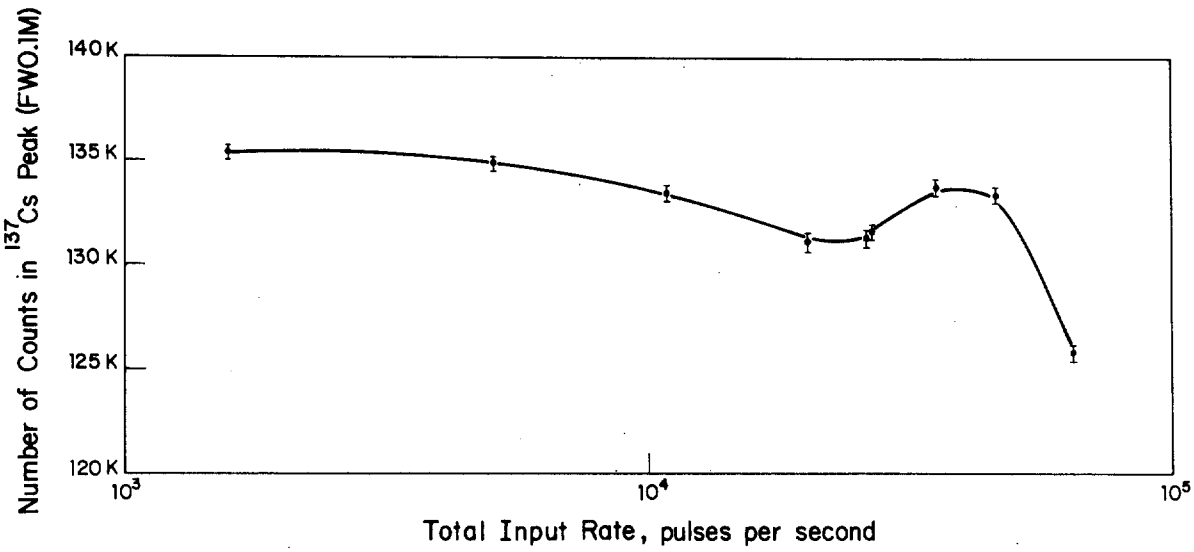

Fig. 4. PHA performance.